

Supporting Information

Complementary Semiconducting Polymer Blends (c-SPBs) for Efficient Charge Transport

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I. OFET Device Fabrication and Characterization

Dichlorobenzene (DCB) solutions of DPP-C0 (3 mg/mL) and DPP-C3 (10 mg/mL) were used as the original solutions. The solution blends with different weight percentages of DPP-C0 were then obtained by mixing the original solutions with different ratio.

For FET devices, a heavily n-doped Si wafer with a 300 nm SiO₂ surface layer (capacitance of 11 nF/cm²) was employed as the substrate with Si wafer serving as the gate electrode and SiO₂ as the dielectric. The gold S/D electrodes were sputtered and patterned by photolithography technique. The device channel length was 50 μm, and the channel width was 1400 μm. For the octadecyltrichlorosilane (OTS) modification, the silicon wafer (with Au bottom contact) was first cleaned with hot piranha solution (H₂SO₄ (98%): H₂O₂ (30% water solution) = 7 : 3). It was then further subjected to sonication sequentially in water and acetone for 6 min each. After drying at an oven, the silicon wafer was then put in a petri dish with a small drop of OTS. The dish was then covered and heated in a vacuum oven at 120 °C for 3 h resulting in the formation of an OTS self-assembled monolayer on the surface. The OTS modified substrates were rinsed successively with hexane, ethanol, and chloroform, and dried by nitrogen. The semiconductor layer was deposited on the OTS-treated Si/SiO₂ substrates by spin coating with spin speed of 2000 r.p.m. and spin time of 90 s. The devices were then annealed in nitrogen glovebox at 150 °C for 10 minutes.

Device characterization of the fabricated polymer blend FETs in room temperature was carried out using Keithley 4200 in ambient air. The field-effect mobility was calculated in the saturation regime by using the equation $I_{DS} = (\mu WC_i/2L)(V_G - V_T)^2$, where I_{DS} is the drain–source current, μ is the field-effect mobility, W is the channel width, L is the channel length, C_i is the capacitance per unit area of the gate dielectric layer, V_G is the gate voltage, and V_T is the threshold voltage.

Low temperature characterization of polymer blend FETs was carried out using Keithley 2400 along with Lakeshore probe station in high vacuum ($<1 \times 10^{-3}$ Pa). Liquid nitrogen was used as cryogenic liquid. The measurement was carried out from low temperature (125 K) to high temperature (300 K) and for each temperature point, 30 minutes was waited to get the temperature stabilized.

II. Supporting Figures and Discussions

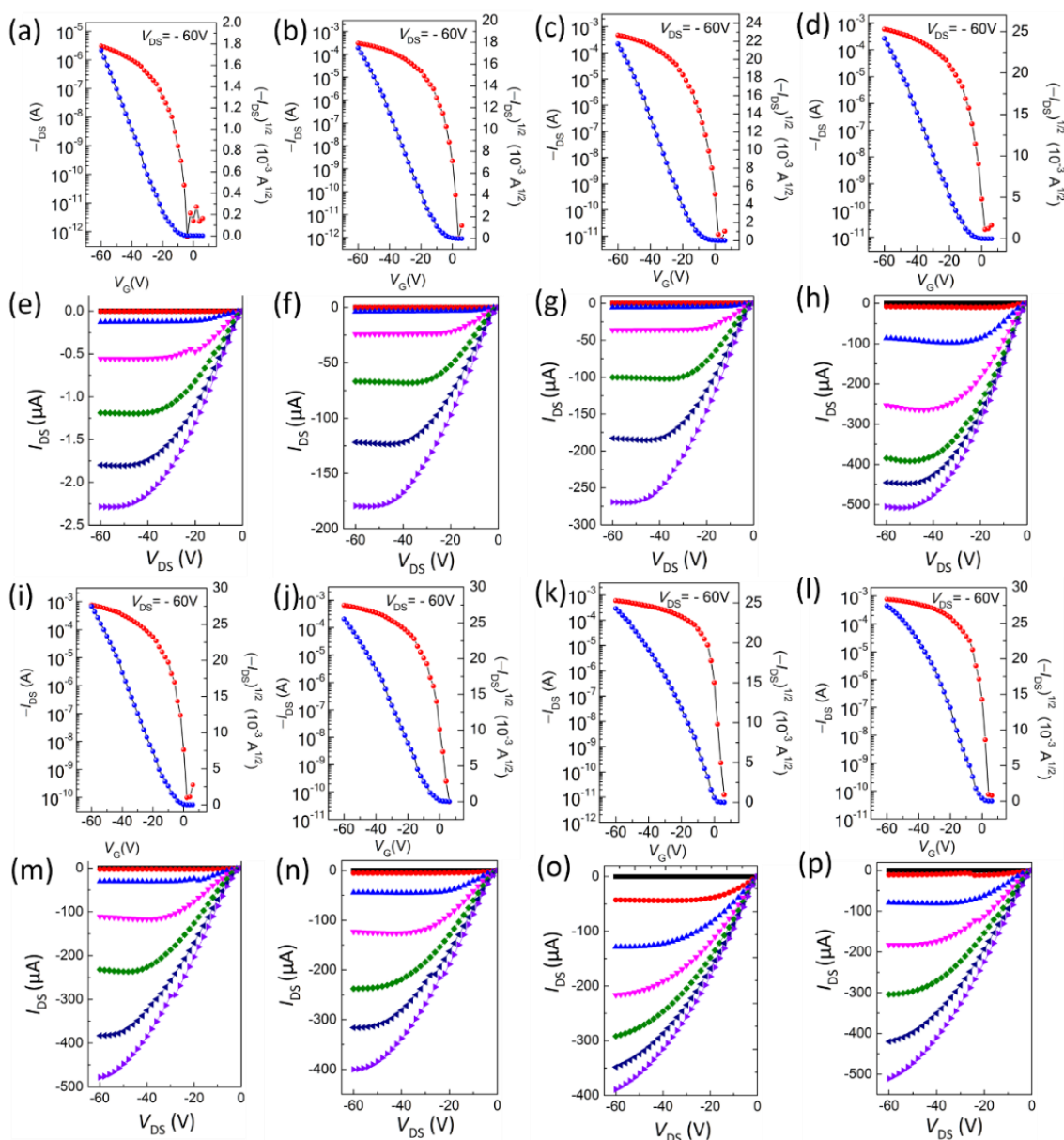


Fig. S1. Transfer and output characteristics of polymer blend FETs. a), b), c), d), i), j), k) and l) are transfer curves for 0%, 1%, 5%, 10%, 30%, 50%, 70% and 100 % of DPP-C0 in DPP-C0/DPP-C3 polymer blend FETs, respectively. e), f), g), h), m), n), o) and p) are transfer curves for 0%, 1%, 5%, 10%, 30%, 50%, 70% and 100% of DPP-C0 polymer blend FETs, respectively. The V_G was set from 0 V to -60 V in steps of -10 V for all output testing.

Table S1. The activation energies for polymer blend FETs and the adjusted R-Square of the linear fit used to calculate the activation energies.

DPP-C0:DPP-C3	E_A (meV)	μ_0	Adj. R-Square
0:100	100.1	0.67	0.98114
1:99	64.63	3.12	0.96621
5:95	61.53	3.41	0.96206
10:90	60.92	3.51	0.9708
30:70	59.37	3.59	0.97129
50:50	57.64	3.46	0.9755
70:30	54.97	4.03	0.96548
100:0	50.48	4.31	0.90089

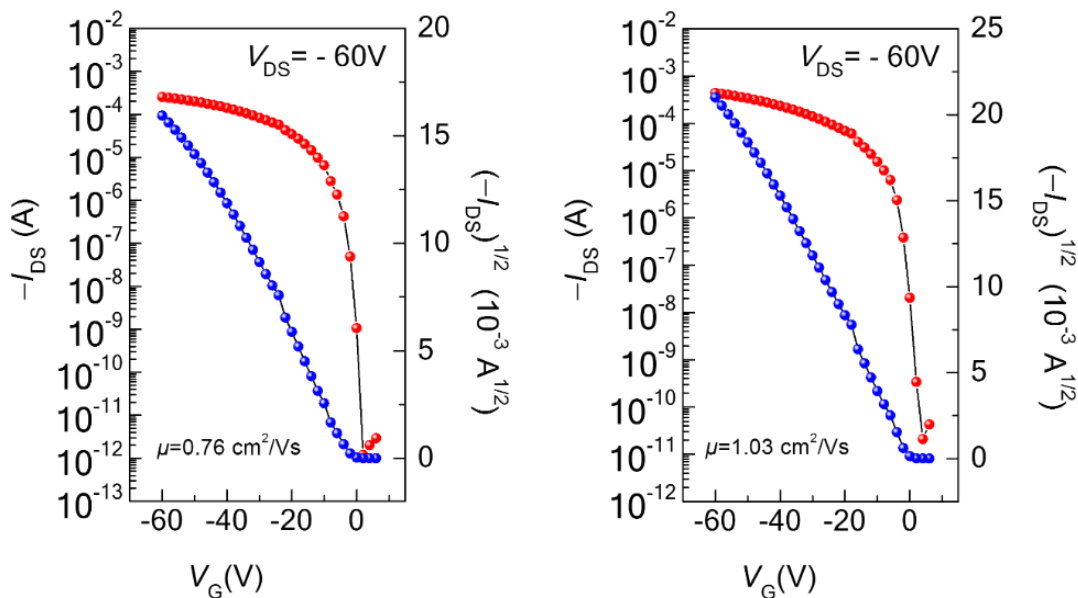


Fig. S2. Transfer characteristic of DPP-C0/PS blend with 1 wt% (left) and 5 wt% of DPP-C0 (right). The annealing temperature is 100 °C.

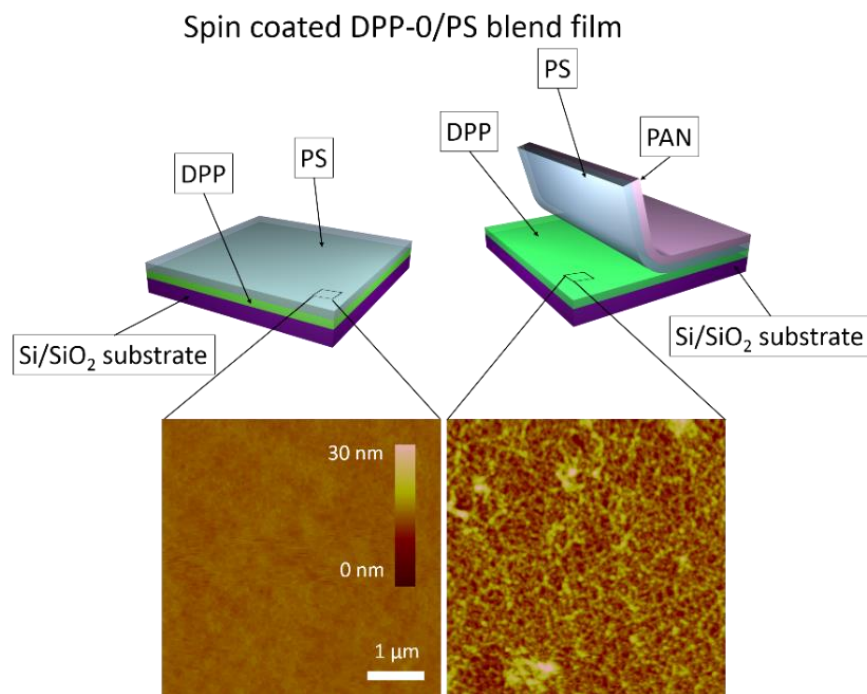


Fig. S3. Schematic drawings and AFM images of spin coated DPP-C0/PS blend thin films with 5 wt% of DPP-C0. Vertical phase segregation is observed by peeling off the PS layer with Polyacrylonitrile (PAN) thin film. The AFM images show clearly different morphologies of PS and DPP-C0 layers.

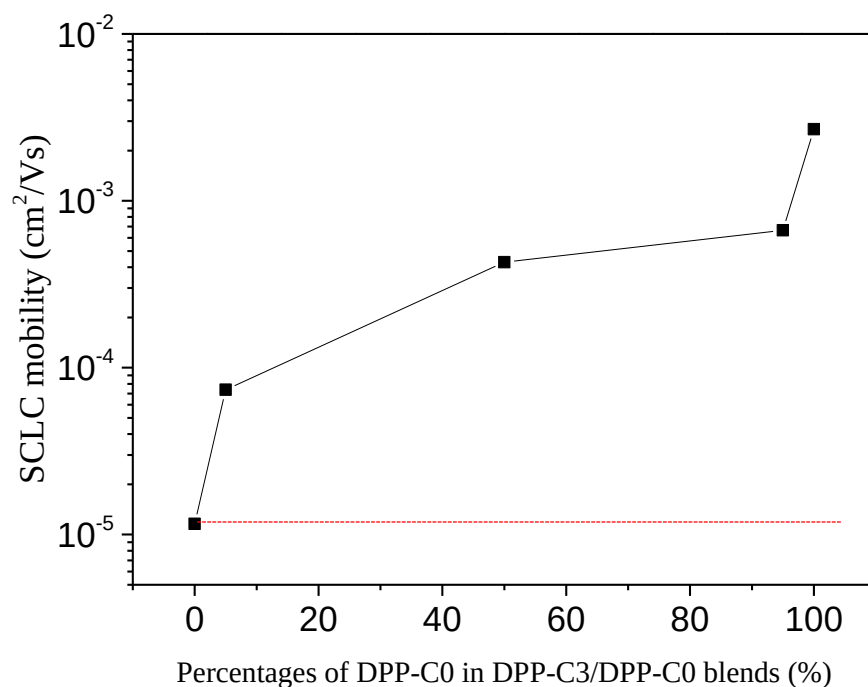


Fig. S4. The plot of SCLC mobility of polymer blend thin films with different ratio of DPP-C0. (Note: if there does exist a vertical phase segregation, one would expect the relationship between SCLC mobility and DPP-c0 ratio follows the red dash line. Instead, we observed the solid black line between them.)

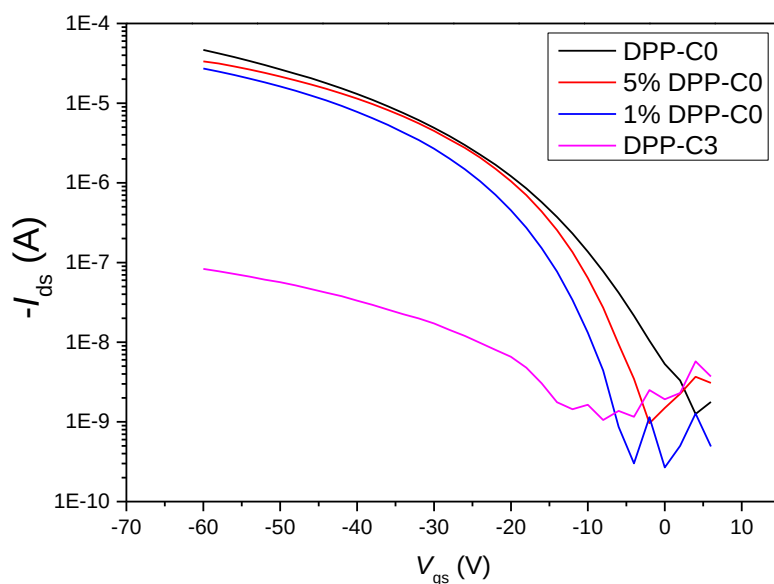


Fig. S5. Transfer characteristics of devices of the top side of delaminated DPP-C0/DPP-C3 blend thin films. Please see previous work (Zhang, L.; Di, C. A.; Zhao, Y.; *et al. Adv. Mater.* **2010**, 22 (32), 3537-41.) for delamination method.

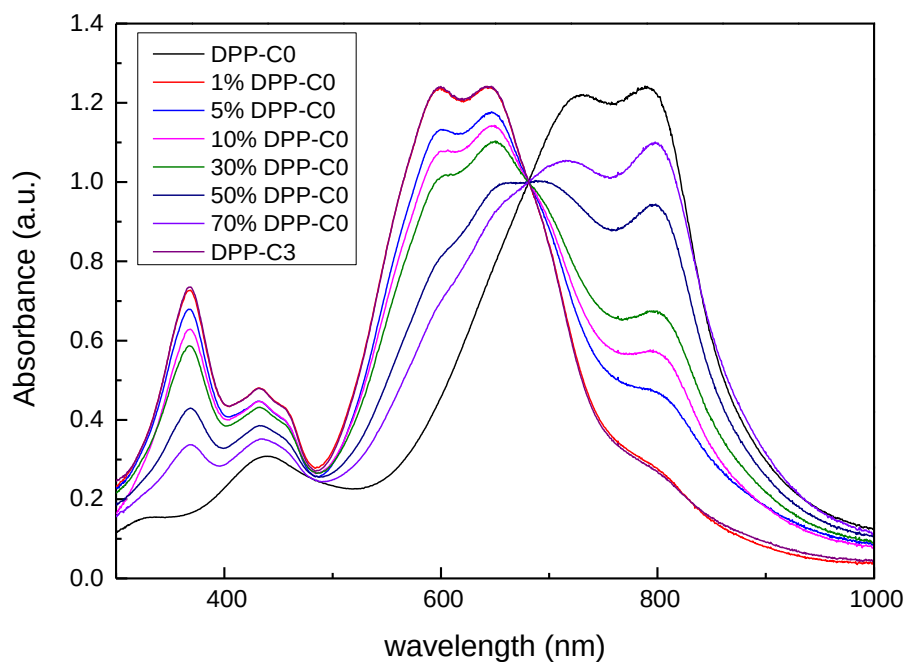


Fig. S6. UV-Vis-NIR spectra of DPP-C3/DPP-C0 blend thin films. The absorbance was normalized at wavelength of 681 nm. (Note: this Figure describes the absorption response with adding the tie chain polymer DPP-C0 into the matrix polymer DPP-C3. At 1 wt%, the spectra for DPP-C3 and the blend are nearly identical, suggesting that DPP-C0 is very dilute in the blend.

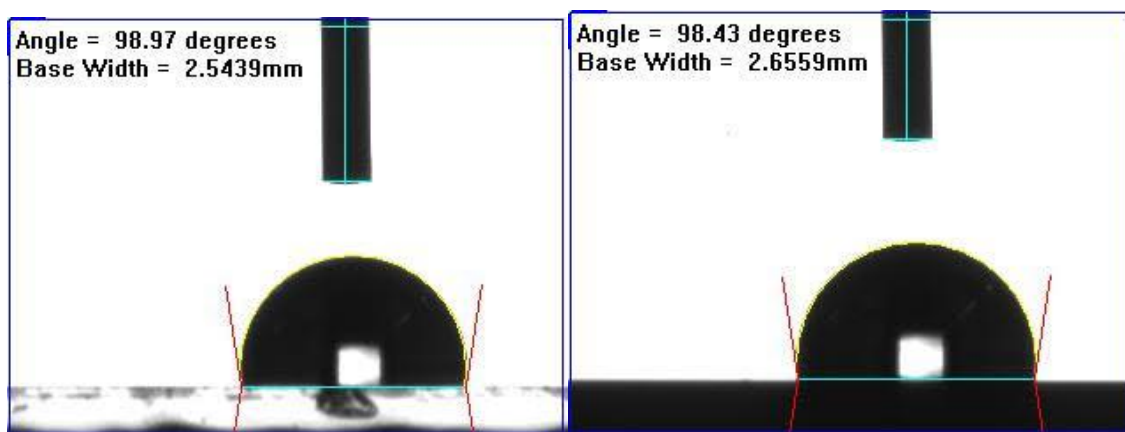


Fig. S7. Contact angles of the DPP-C0 (left) thin film and the DPP-C3 (right), respectively. This experiment was suggested by a reviewer to evaluate whether there is a vertical phase segregation in the polymer blends. We found out that the contact angles are too similar for two polymers. It is not an effective approach. Nevertheless, we put the results here.