

ADVANCED MATERIALS

Supporting Information

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Melt-Processing of Complementary Semiconducting Polymer
Blends for High Performance Organic Transistors

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Gumyusenge, Alexander L. Ayzner, and Jianguo Mei**

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Experimental details

Material preparation. DPP-C0 (3.3 mg/mL) and DPP-C5 (10 mg/mL) were dissolved in dichlorobenzene at 50 °C stirred overnight. The *c*-SPB solution were obtained by mixing the 5 wt% of DPP-C0 solutions into 95 wt% of DPP-C5 solutions. Before use, the DPP-C0 solution was stirred and heated up to 50 °C. The *c*-SPB solid was dried from its solutions.

Melt-processed thin film fabrication. Solution-based OTS-modification was used to prepare the substrates for melt processing. The DPP-C5 and *c*-SPB materials are sticky to glass or bare silicon wafer and hard to peel-off, thus the OTS-modification is essential for peel-off process. The SiO₂/Si substrates were first cleaned with hot piranha solution (H₂SO₄ (98%) : H₂O₂ (30% water solution) = 7 : 3) for 20 minutes. They were then washed with deionized (DI) water several times, and further subjected to sonication sequentially in DI water and acetone for 6 min each. After drying inside an oven, the substrates were put into freshly prepared OTS solution (OTS : hexane = 1 : 1000, v : v) directly for 5 min. The substrates were then washed with pure hexane and dried by nitrogen gas. For film fabrication, the DPP-C5 or *c*-SPB materials was put between to OTS-modified substrates on a hot plate. After the materials get melted, a heavy object (~ 4 kg) was put on top of the substrates to press the materials. With different press time and temperatures, different film thickness can be achieved. For peel-off process, the two substrates were first separated. The film was then peeled off, starting from the corner or the edge of the substrate.

FET device Fabrication. A heavily n-doped Si wafer with a 300 nm SiO₂ surface layer (capacitance of 11 nF/cm²) was employed as the substrate with Si wafer serving as the gate electrode and SiO₂ as the dielectric. The gold S/D electrodes were sputtered and patterned by photolithography technique. For the vapor-based octadecyltrichlorosilane (OTS) modification, the silicon wafer (with or without Au bottom contacts) were first cleaned with hot piranha solution for 20 minutes. It was then washed with deionized (DI) water several times, and further subjected to sonication sequentially in DI water and acetone for 6 min each. After drying inside an oven, the silicon wafer was then put into a clean petri dish with a small drop of OTS. The dish was then covered and heated in a vacuum oven at 120 °C for 3 hours, resulting in the formation of an OTS self-assembled monolayer on the surface. The OTS modified substrates were rinsed successively with hexane, ethanol, and chloroform, and dried by nitrogen. The semiconductor layer was deposited on the OTS-treated Si/SiO₂ substrates by spin coating with spin speed of 1500 rpm. and spin time of 120 s. The devices were then annealed in nitrogen glovebox. For DPP-C0 and *c*-SPB OFETs, the channel length was 60 μm and channel width was 1000 μm. For DPP-C5, the channel length was 5 μm and channel width was 1000 μm.

Electrical characterization. Device characterization was carried out using Keithley 4200 for all testing. For spin-coated and hot-pressed *c*-SPB OFETs, the electrical measurement was carried out at room temperature in ambient air. For the temperature-dependent OFET performance, a microscope hot stage was used to precisely control the temperature both in ambient air and inside nitrogen glovebox. The field-effect mobility was calculated in the saturation regime by using the equation $I_{DS} = (\mu WC_i/2L)(V_G - V_T)^2$, where I_{DS} is the drain-source current, μ is the field-effect mobility, W is the channel width, L is the channel length, C_i is the capacitance per unit area of the gate dielectric layer, V_G is the gate voltage, and V_T is the threshold voltage. Three batches of devices and more than 4 devices in each batch were tested, and their results were in good agreement. Temperature-dependent electrical measurement was carried out on a Caikang CK-300/400 hot plate both inside and outside of N₂ glovebox. The heating rates were kept around 0.5 °C/s. We also allowed the sample to equilibrate for 1 minutes before taking electrical measurement.

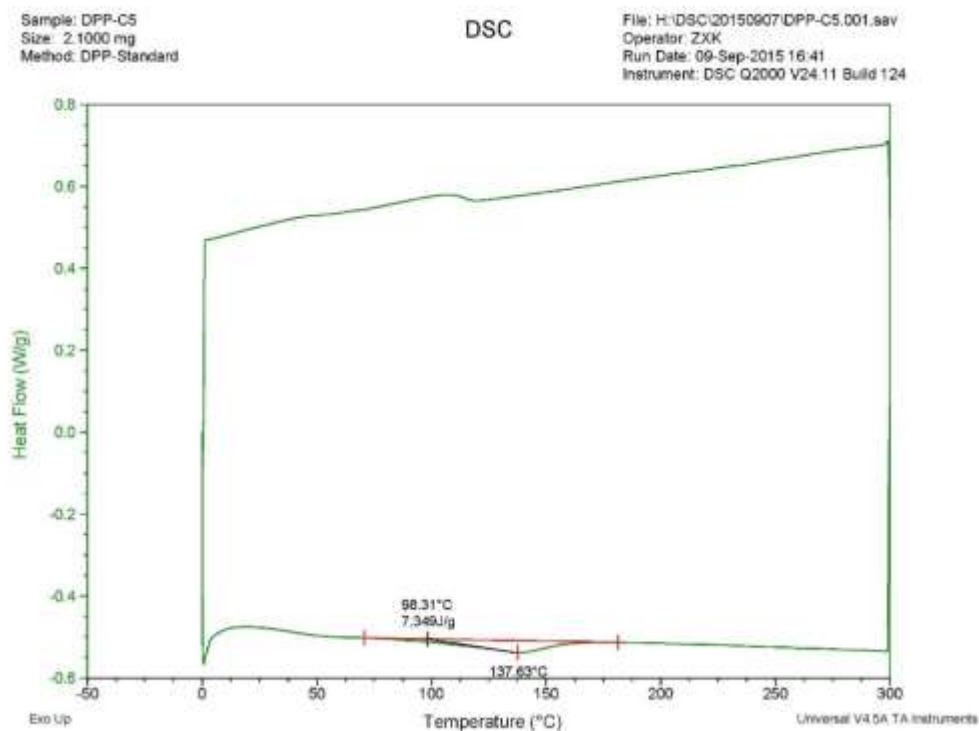


Figure S1 Differential scanning calorimetry (DSC) curves of DPP-C5.

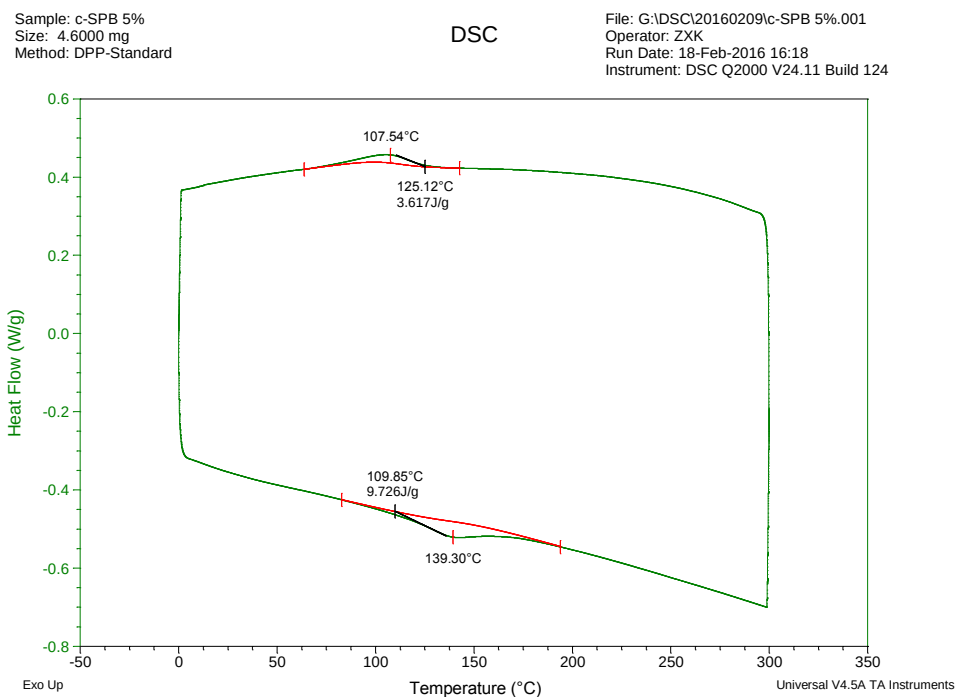


Figure S2 DSC curves of the *c*-SPB blend.

Table S1. Time and temperature effects for film thickness. (5 wt% of DPP-C0 in *c*-SPBs and 10 KN/cm² are used for all experiments.)

	Film thickness (μm)		
	15 min	30 min	60 min
160 °C	1.92	1.67	1.54
180 °C	0.99	0.95	0.94

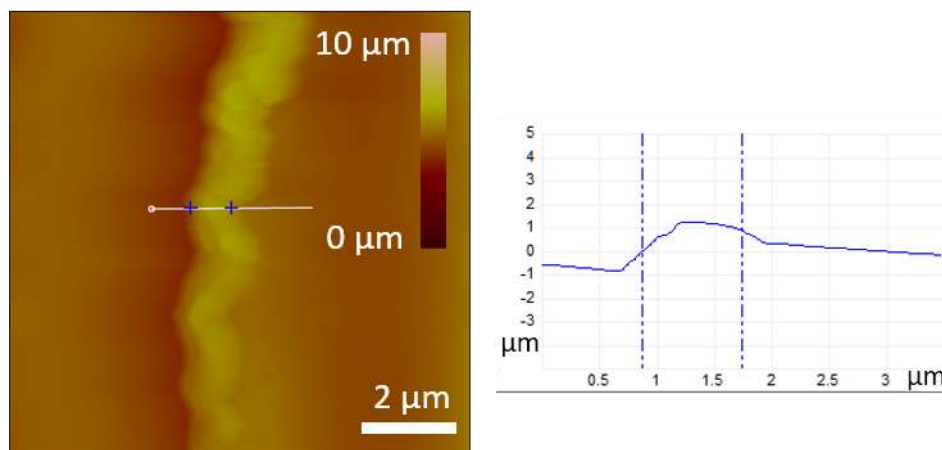


Figure S3 Thickness of melt-processed *c*-SPB thin film measured by AFM.

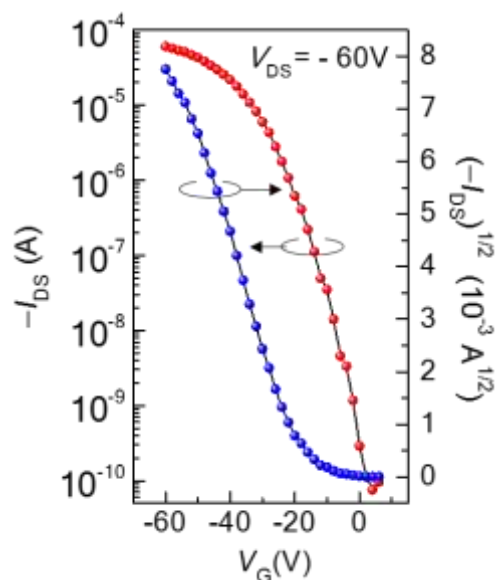


Figure S4 The transfer characteristic of the device made by direct melt processing approach. The channel length of this device is 50 μm and channel width is 1400 μm . The mobility is 0.31 cm²/Vs. (see ref. 18 for devices fabrication details)

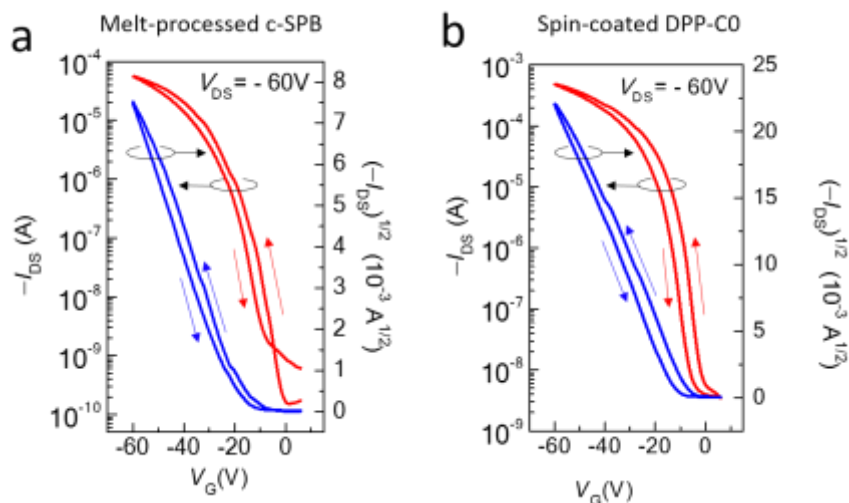


Figure S5 Hysteresis measurement for (a) melt-processed *c*-SPBs (by peel-off and transfer approach) and (b) spin-coated DPP-C0 OFETs. The V_G was scanned from 6 V to -60 V with 2 V step, and then scanned back from -60 V to 6 V. The scan speed was 10 V/s.

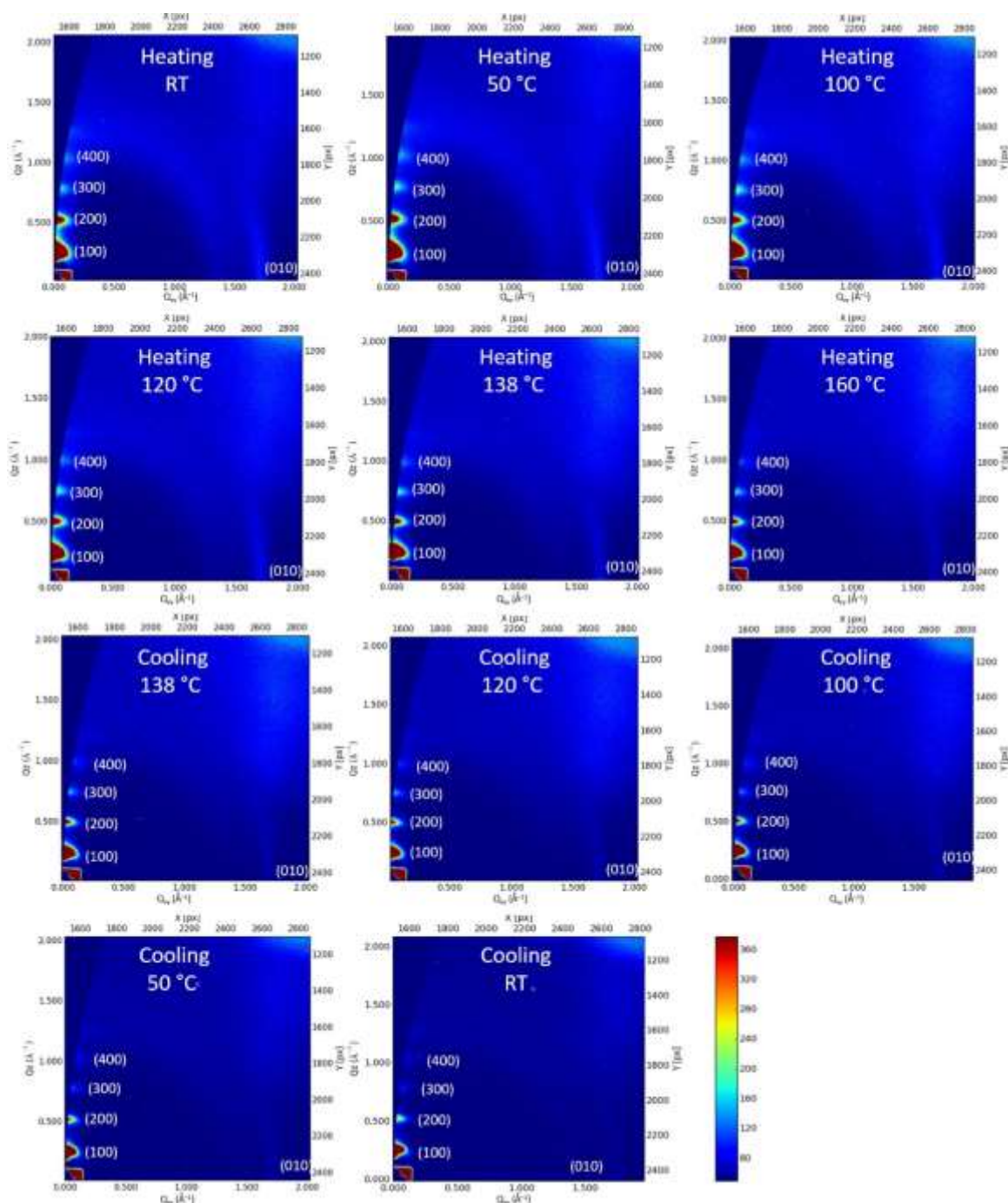


Figure S6 In-situ temperature-dependent GIXRD measurements of DPP-C0 thin. The thin film was prepared on OTS-modified Si/SiO₂ substrate by spin coating. Before measurement, the thin film was annealed at 120 °C for 10 min in glovebox.

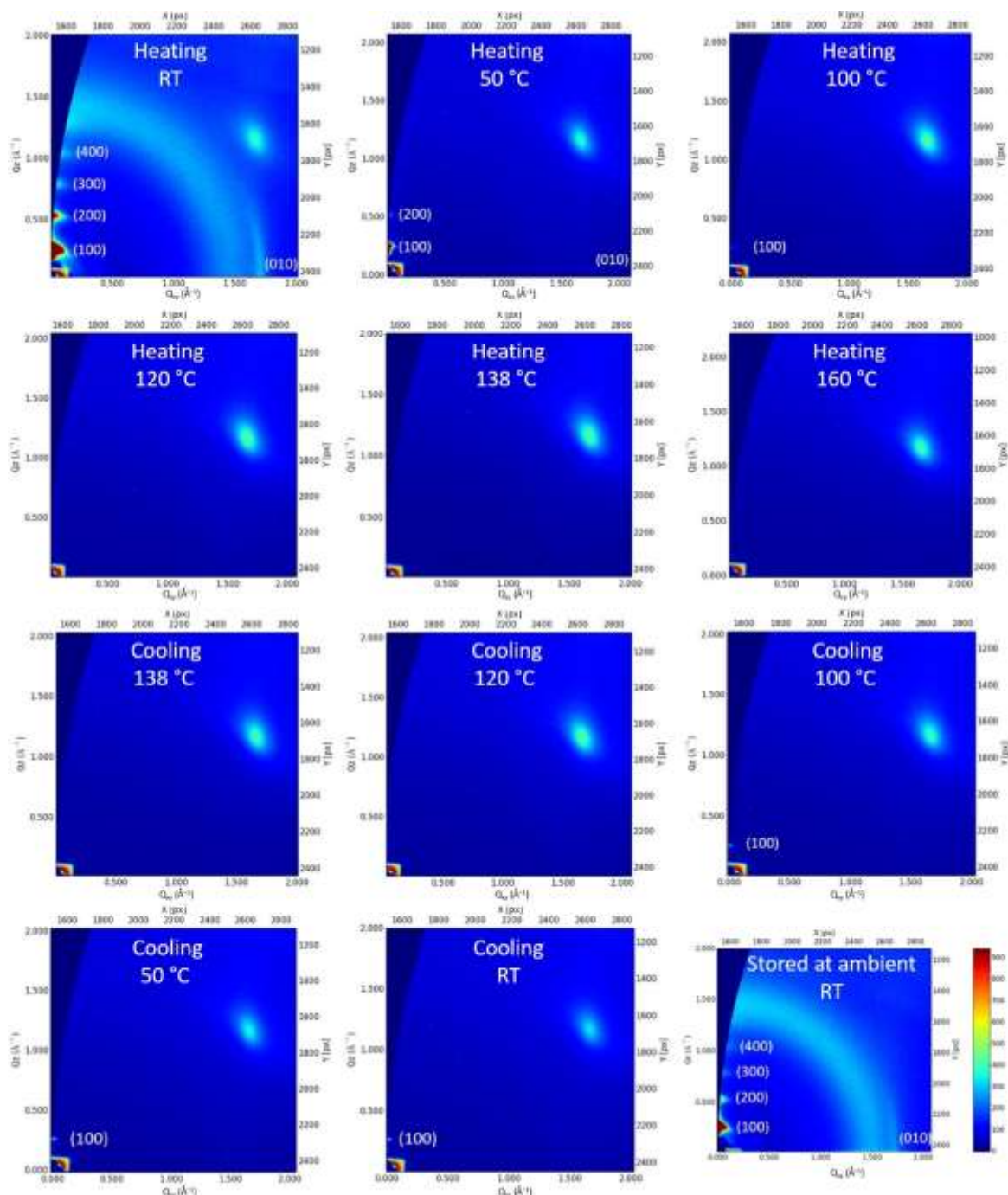


Figure S7 In-situ temperature-dependent GIXRD measurements of DPP-C5 thin film. The thin film was prepared on OTS-modified Si/SiO₂ substrate by spin coating. Before measurement, the thin film was annealed at 120 °C for 10 min in glovebox. The bright spot in the right part of the pattern is an artifact of the silicon substrate. The presence of the spot depends on the orientation of the sample with respect to the incoming x-ray and the detector.

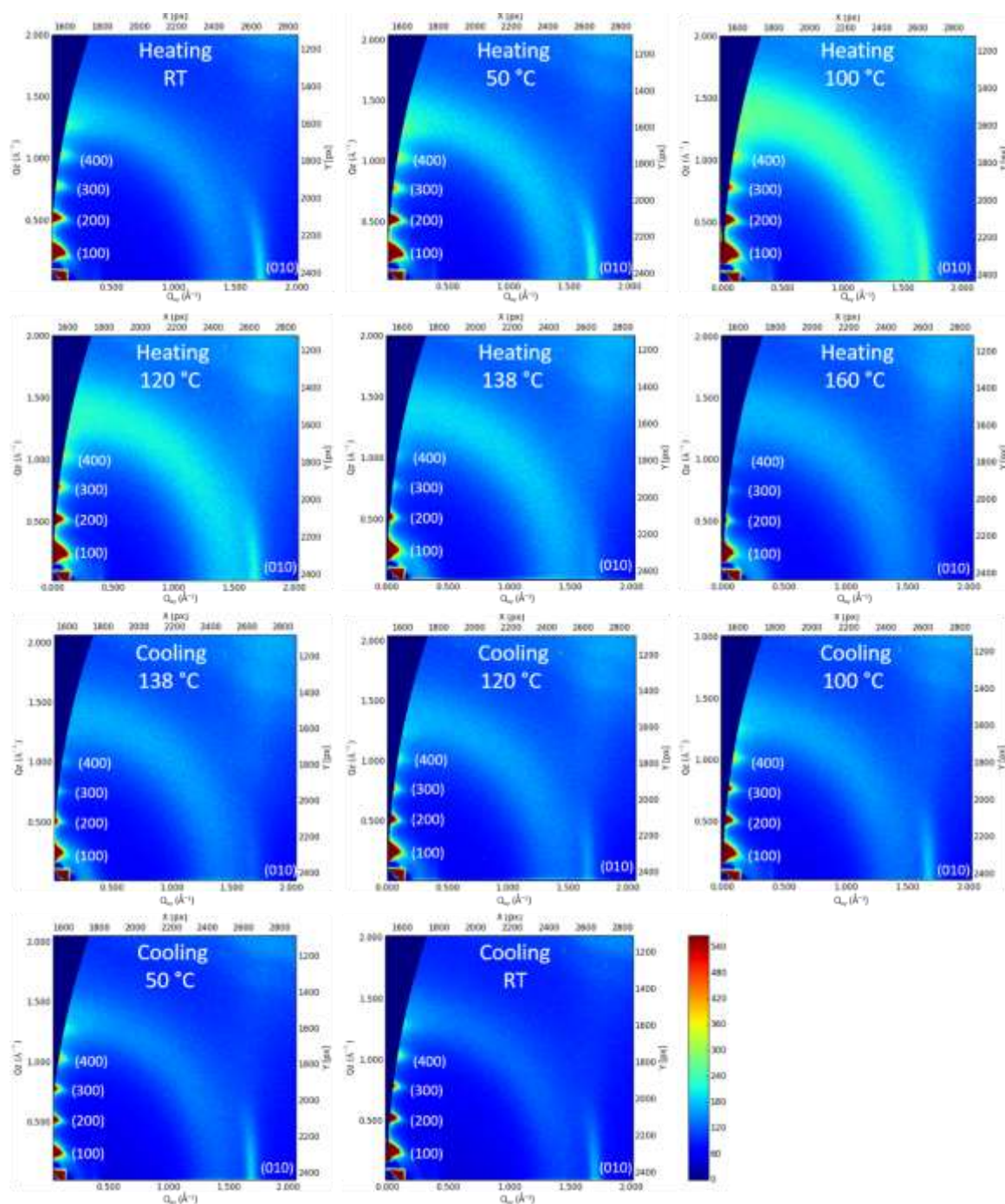


Figure S8 In-situ temperature-dependent GIXRD measurements of c-SPB thin film. The thin film was prepared on OTS-modified Si/SiO₂ substrate by spin coating. Before measurement, the thin film was annealed at 120 °C for 10 min in glovebox.

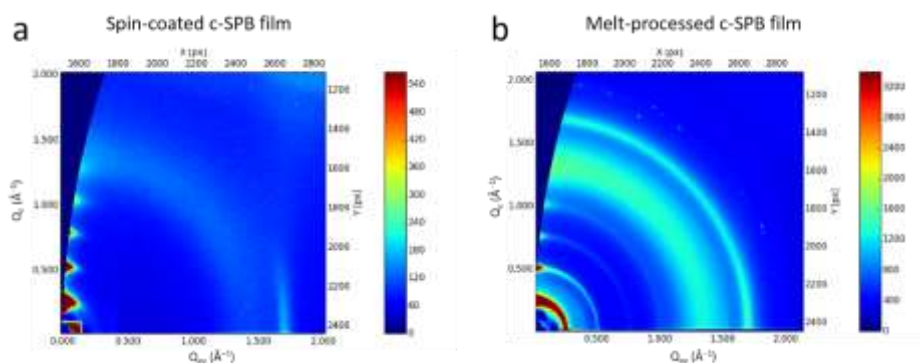


Figure S9 GIXRD pattern of (a) spin-coated and (b) melt-processed *c*-SPB films.

We chose spin-coated thin films for the in-situ temperature GIXRD experiments, instead of free-standing melt-processed films. Because they are usually thick ($\sim 1\ \mu\text{m}$) and are not suitable for the GIXRD measurements to reveal the chain orientation information at the interface. First, GIXRD is a thickness sensitive technique. We would not be able to get the information on the microstructure at the interface of semiconductor layer/dielectric layer, which determines the charge transport behaviors. Second, we like to make a comparison among DPP-C0, DPP-C5, and *c*-SPB films and investigate the impact of DPP-C0 chains in the *c*-SPB. Unfortunately, DPP-C0 cannot be melt processed to get a film. Third, we ran the GIXRD experiments as high as $160\ ^\circ\text{C}$, higher than the melting temperatures of DPP-C5 and the *c*-SPB. In other words, the melting behaviors of these materials can be still revealed. For a discussion of GIXRD measurements on melt-processed thick film, one can refer to our previous work (Conjugation-Break Spacers in Semiconducting Polymers: Impact on Polymer Processability and Charge Transport Properties, *Macromolecules*, **2015**, 48, 2048–2053).

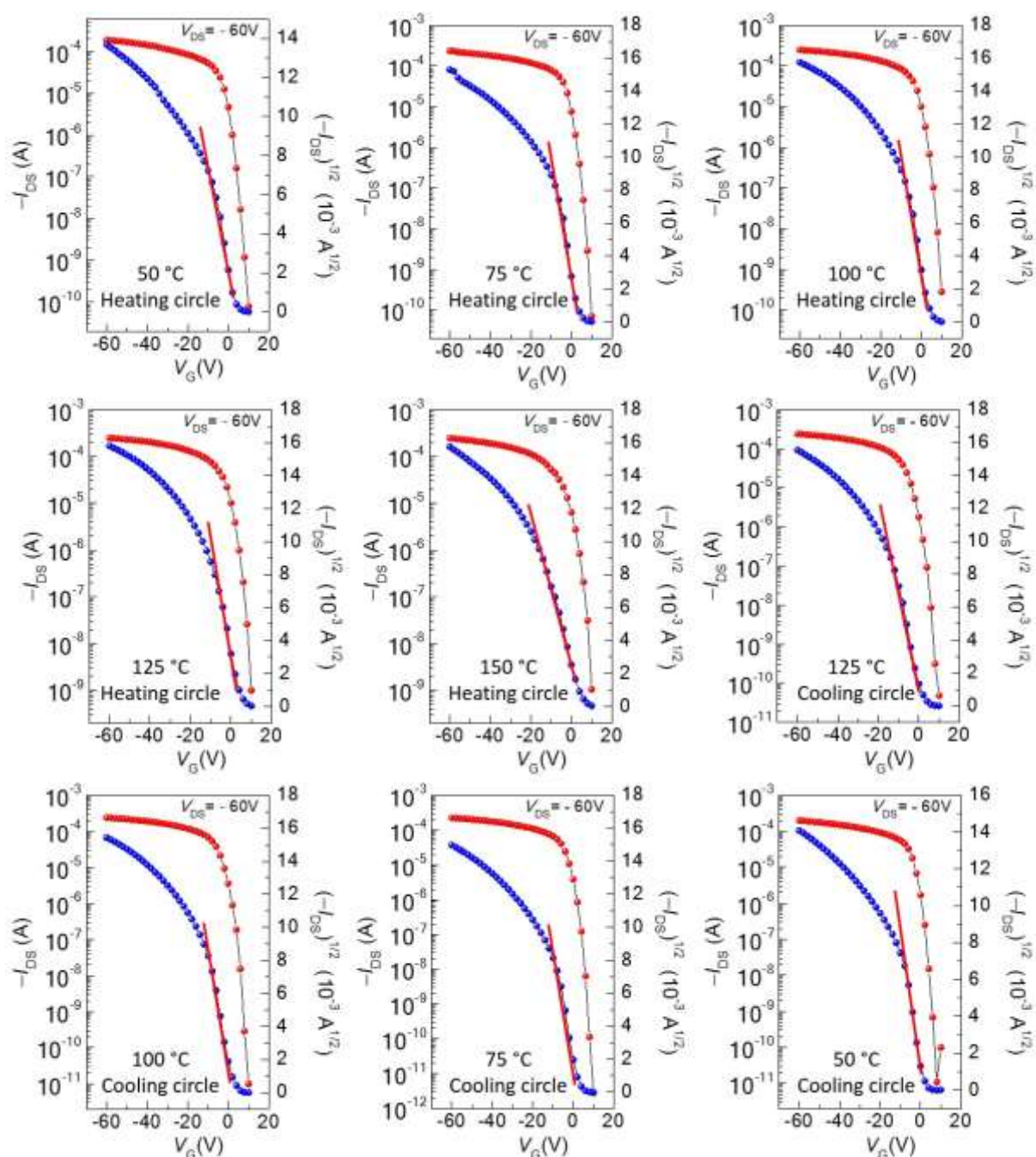


Figure S10 Transfer characteristics of DPP-C0 OFETs at different temperature.

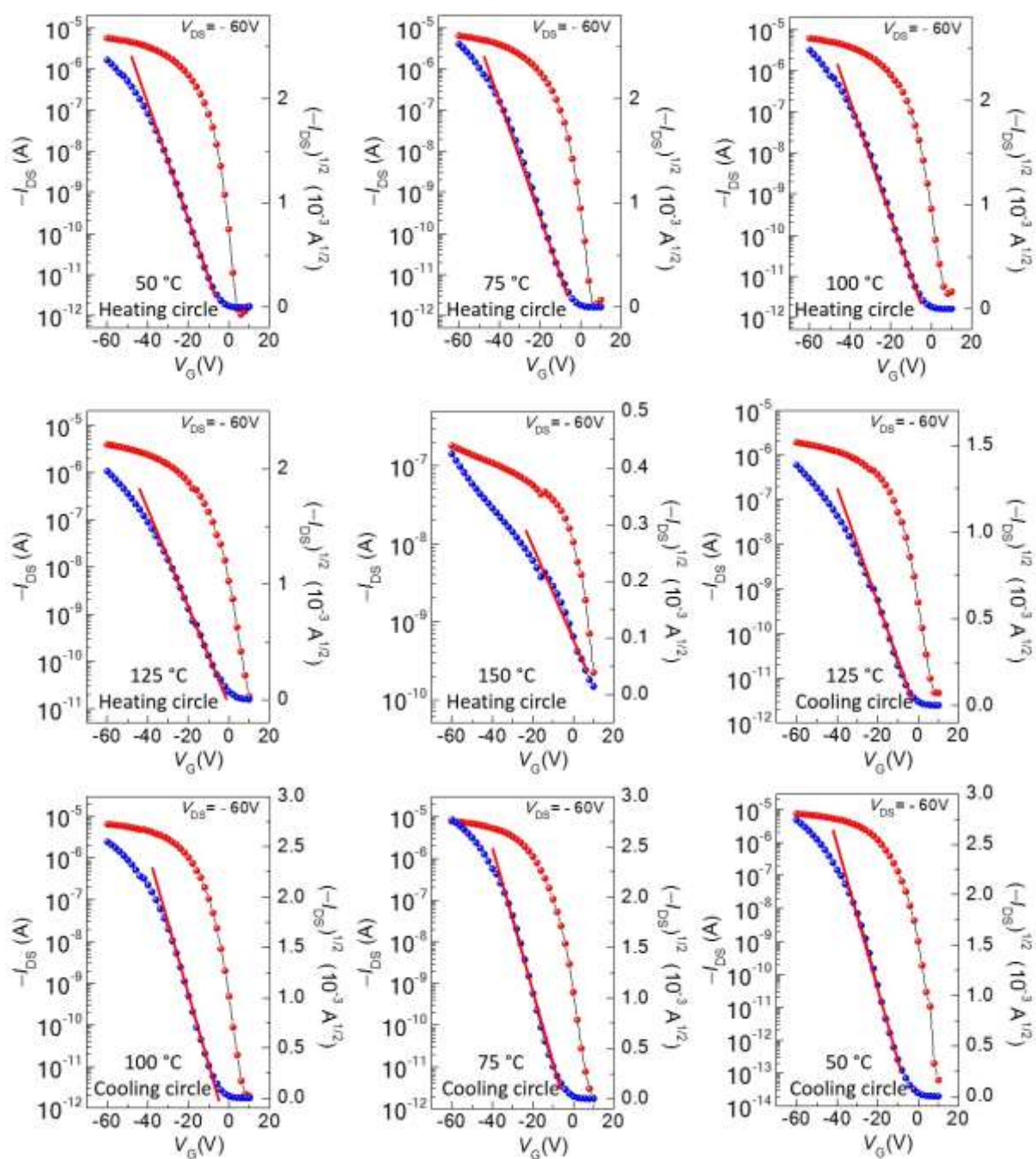


Figure S11 Transfer characteristics of DPP-C5 OFETs at different temperature tested in N₂ glovebox.

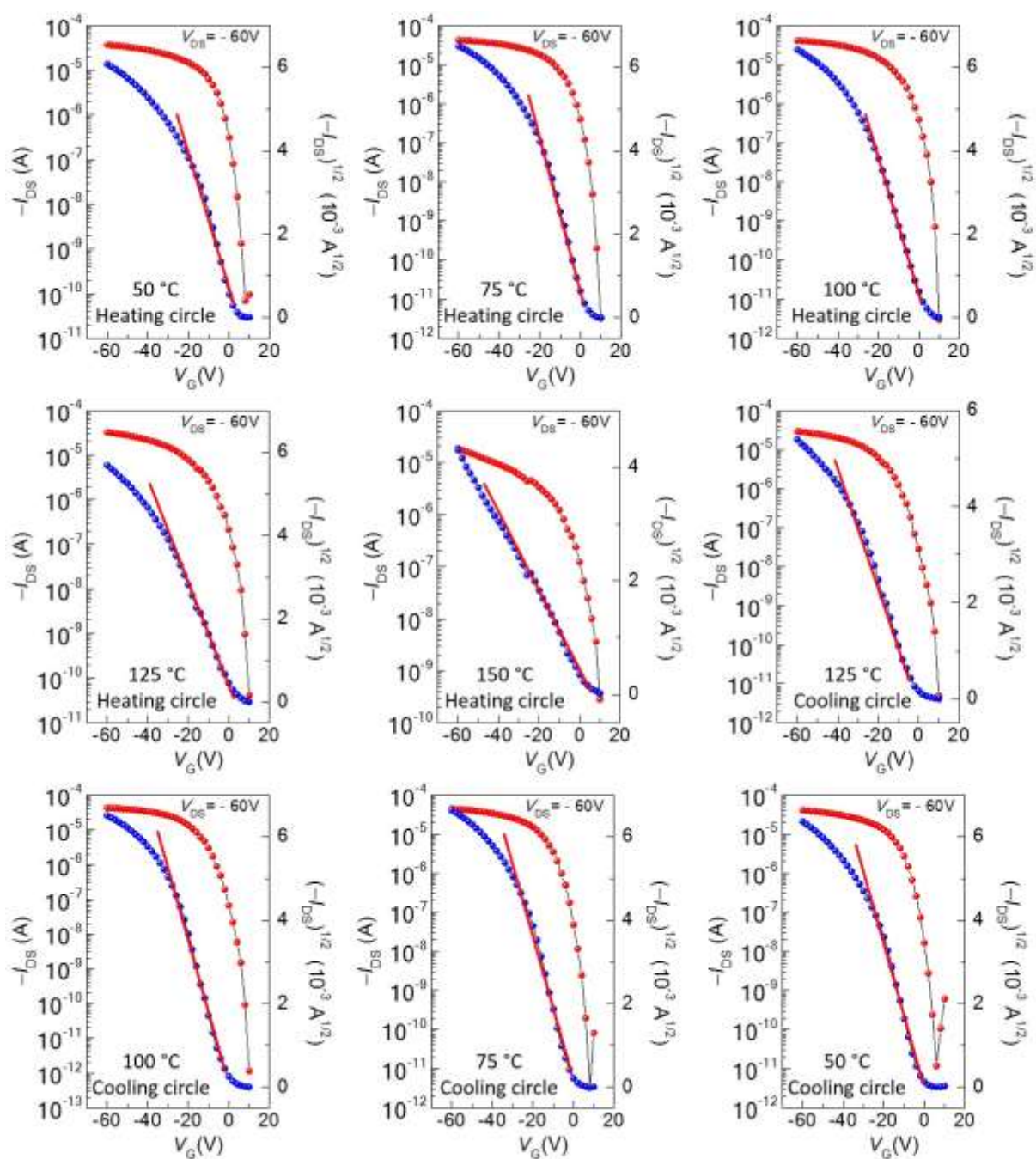


Figure S12 Transfer characteristics of *c*-SPBs OFETs at different temperature tested in N₂ glovebox.

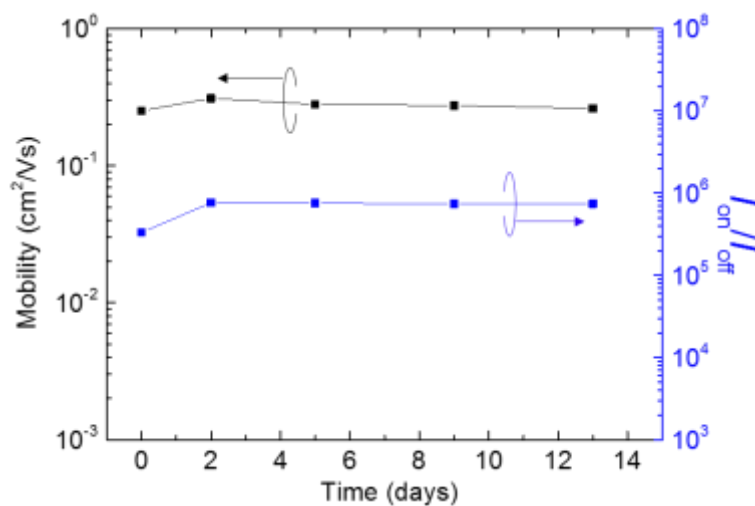


Figure S13 Stability test of melt-processed *c*-SPBs OFETs. The OFET measurement was carried out in the ambient air. After measurement, the device was stored in a N₂ filled glovebox. The channel length is 50 μ m and channel width is 1400 μ m.

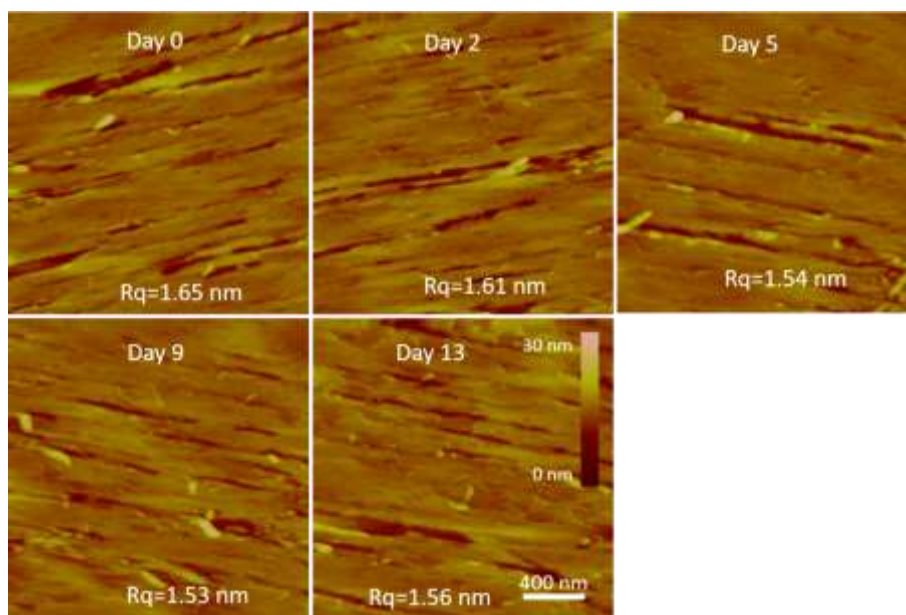


Figure S14 Morphological stability of melt-processed *c*-SPBs thin film measured by AFM.

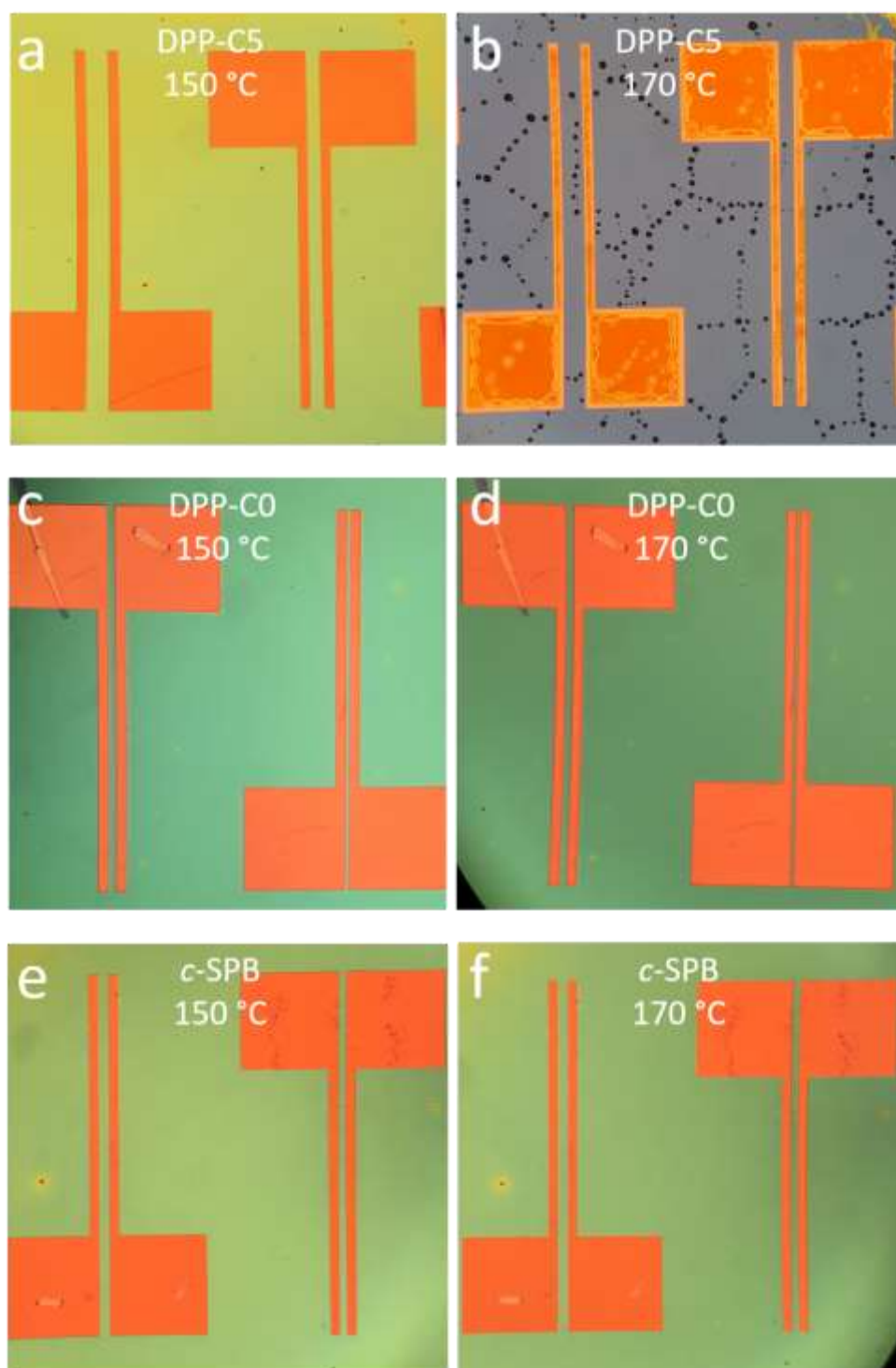


Figure S15 Optical images of DPP-based polymer thin films at 150 °C and 170 °C. (a) DPP-C5, (c) DPP-C0 and (e) *c*-SPB thin films at 150 °C. (b) DPP-C5, (d) DPP-C0 and (f) *c*-SPB thin films at 170 °C. The substrates are OTS-modified Si/SiO₂ with Au contacts.

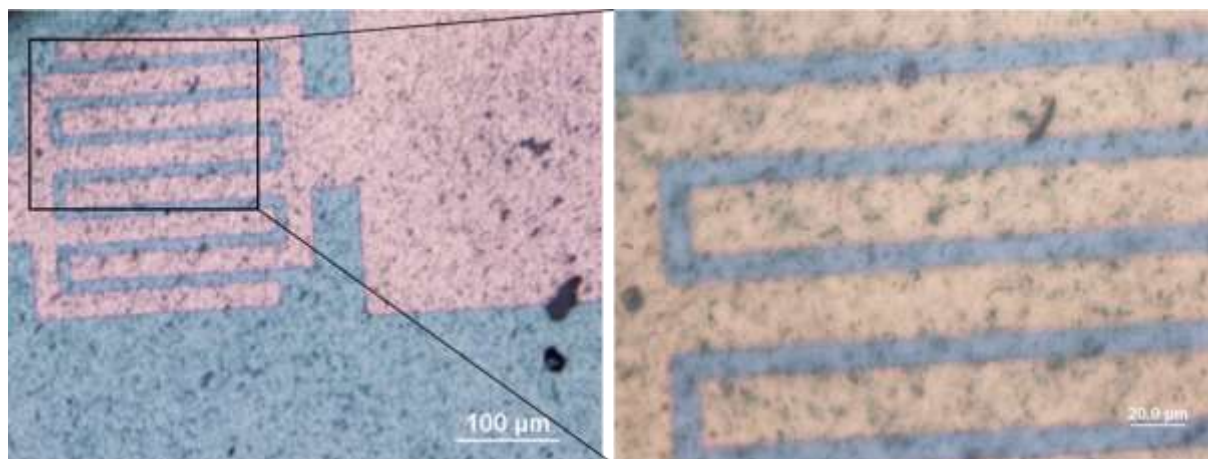


Figure S16 Optical microscope images of melt-processed DPP-C0/PS blend film and the OFET device. It shows clearly that there is phase segregation between PS and DPP-C0, and the DPP-C0 phase is discontinuous.

DPP-C0/PS blend thin film and device fabrication. 950 μL PS solution (10 mg/mL in DCB) was mixed with 100 μL DPP-C0 solution (5 mg/mL in DCB) to get 5 wt% DPP in DPP-C0/PS polymer blend. The polymer blend solution was then dried in N₂ glovebox at 70 °C to get the polymer blend solid material. The solid material was directly used for OFET devices. For melt-processed OFETs, the polymer blend solid was put on a clean glass or silicon substrates on a hot plate. After the polymer blend melted at 220 °C, an OTS modified SiO₂/Si wafer was covered from top of the melted polymer. The silicon wafer was then pushed to one direction to obtain the polymer film. The devices were then tested in the open air ($V_{ds} = -60$ V, V_g from 10 to -60 V). No OFET preference was observed.

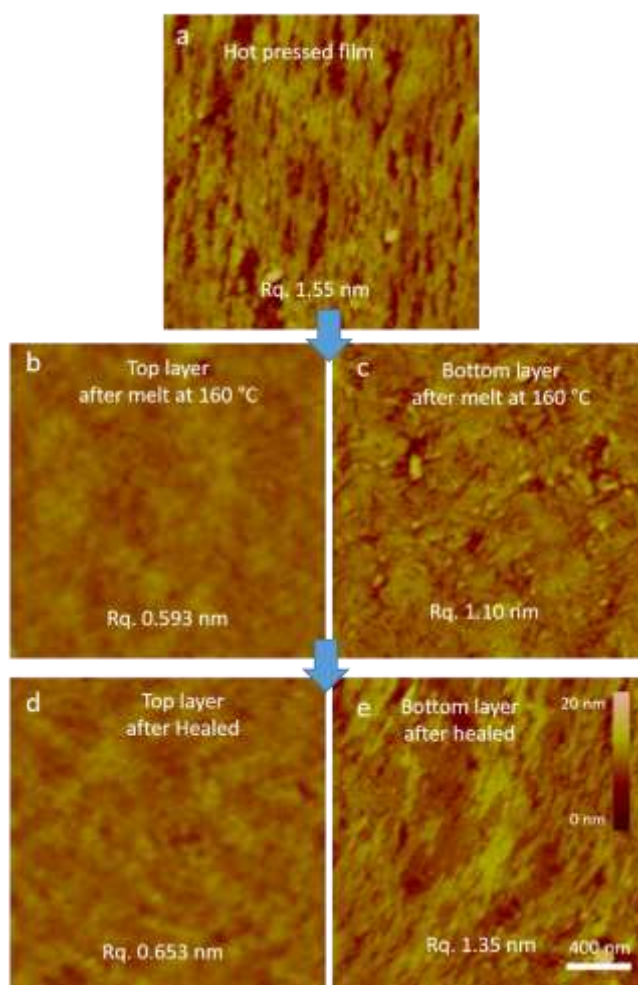


Figure S17 AFM images of *c*-SPB thin films. (a) Melt-processed *c*-SPB thin film. (b) Top surface of melt-processed film after melt at 160 °C. (c) Bottom surface of melt-processed film (by peel-off approach) after melt at 160 °C. (d) Top surface of the scratched area after “melt-heal-cool down” approach. (e) Bottom surface of the scratched area (by a peel-off approach) after “melt-heal-cool down” approach.