

Supporting Information for:

Polyimide-based High Temperature Plastic Electronics

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1) Experimental Section

Materials: Kapton® HN (100 HN and 500 HN) substrates were obtained from DuPont as a gift and were rinsed by sonicating for 5 minutes in hexanes, isopropanol, then acetone prior to usage. Poly(pyromellitic dianhydride-co-4,4-oxydianiline)(PAA) was obtained from Millipore Sigma and used received. Matrimid® 5218 (MI) was purchased from PolyK Technologies and purified by precipitation, filtration, washing with methanol and drying before use. PII-2T was synthesized and purified as reported in our previous works.^{1,2} High purity Au and Al pellets were purchased from Kurt J. Lesker Company and subject to high vacuum before deposition.

OFETs fabrication and characterization: Polyimide substrates were first cut into desired shapes and rinsed in hexanes, isopropanol, then acetone. After nitrogen-drying, the substrates were carefully transferred into a high-vacuum chamber (2×10^{-6} mbar) and Al gates were deposited at an optimal deposition rate of $5.0 \text{ \AA/s}$ to a final thickness of 70 nm with careful heating power tuning required for a stabilized deposition rate. We noted that the deposition rate for Al can be challenging to control, and for thicker deposited gate contacts, more attention had to be paid to the dielectric to ensure full coverage of the gates therefore eliminating any parasitic leakage currents. A film of PAA was then spun onto the Al-covered substrates as previously reported³ (spin rate of 6000 rpms for a minimum of 2 minutes). The substrates were then allowed to heat up to $300 \text{ }^{\circ}\text{C}$ for 1 hour at ambient for a complete imidization and PI film formation. These processing conditions yield 200 nm thick films of PI after curing. After cooling down, the semiconducting layer of PII-2T/Matrimid blend was deposited by spin coating chloroform solution (10 mg/mL, 3000 rpms, 30 s) then annealed at $220 \text{ }^{\circ}\text{C}$ for 30 minutes inside a nitrogen-filled glovebox. For the temperature dependent studies, the 50/50 blend ratio was chosen for the bi-continuous morphology. Au source/drain contacts were then deposited through a prepatterned shadow mask (channel length of $40 \text{ }\mu\text{m}$) at a rate of $1.0 \text{ \AA/s}$ to a final thickness of 30 nm.

OFET devices characterizations were carried out using a Keithley 4200 in ambient environment. The field-effect mobility was calculated in the saturation regime by using the equation $I_{DS} = (WC_i / 2L)\mu(V_G - V_T)^2$, where I_{DS} is the drain-source current, μ is the field-effect mobility, W is the channel width, L is the channel length, C_i is the capacitance per unit area of the gate dielectric layer, V_G is the gate voltage, and V_T is the threshold voltage. A channel area of 1500 μm^2 was carefully isolated (Fig. S5) and a channel length of 40 μm was used for mobility calculations. OFET performances were obtained by applying a gate bias from -15 V to 6 V , with the potential gradient between the source and drain contacts kept at -10 V .

Capacitance measurement: To extract the capacitance of the PI dielectric, polyimide substrates were first cleaned and transferred inside a thermal-deposition chamber. A thin layer of Au was then deposited, followed by spin coating and thermal curing the dielectric layer. Using 1.1 mm x 1.1 mm stainless steel shadow mask, the Au/PI/Au sandwich structure could be achieved. The capacitance was then measured using a GW Instek LCR-6100 Precision LCR Meter in the Au/PI/Au sandwich configuration. The frequency could be varied from 100 Hz to 100 kHz. The capacitance was calculated to be around 4.5 nF/cm² in good agreement with previous reports.^{3,4} To probe the thermal stability of the dielectric layer, the Kapton/Au/PI/Au sandwich assembly was brought to different temperatures and the measurements were taken in ambient air.

In-situ temperature-dependent measurements: To control the thermal conditions both for FETs characterization and capacitance measurements, the HFS600E-PB4 Linkam stage was used with the heating and cooling rates maintained at 10 °C/min and the devices were allowed to reach thermal equilibrium for 30 minutes at each temperature before measuring unless indicated otherwise.

Morphology analysis: The AFM height were obtained using Cypher Asylum AFM and processed through Gwyddion Software. All films were processed on cleaned Kapton substrates

and film morphology was imaged after annealing the blend onto top of the imidized PI film. To extract the thickness, a sharp probe tip was used to form a notch through the thermally cured film or the semiconducting blend film.

2) Dielectric film thickness and capacitance evaluation

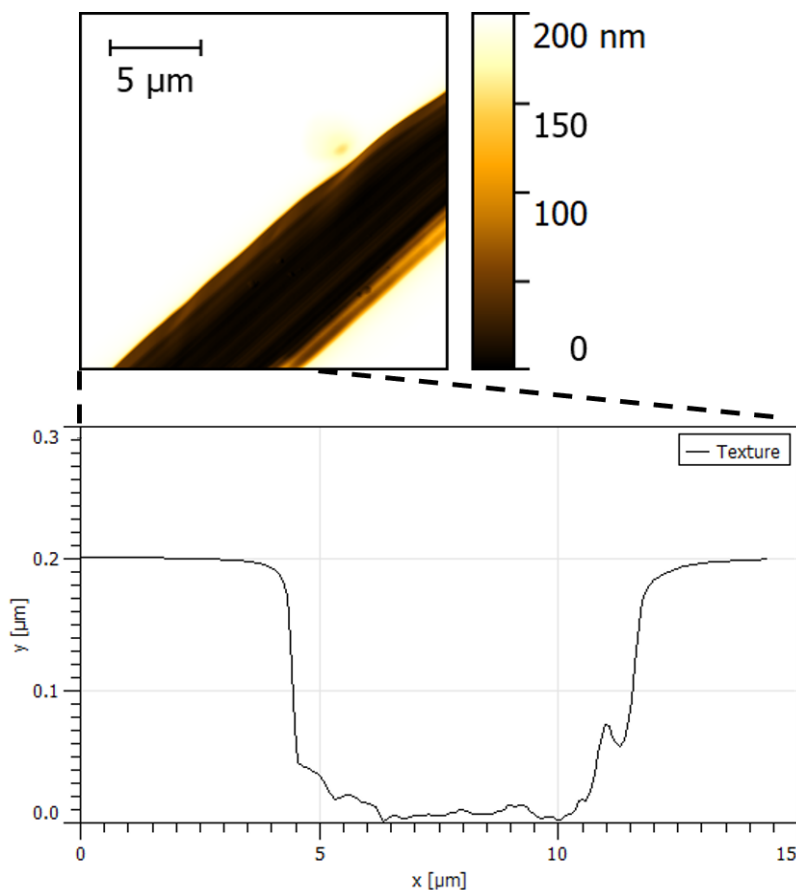


Figure S1. Thickness evaluation of the thermally-cured PI film using AFM. A deep notch was carefully created through the film using a probe tip. The overall film thickness was measured to be around 200 nm (± 10 nm).

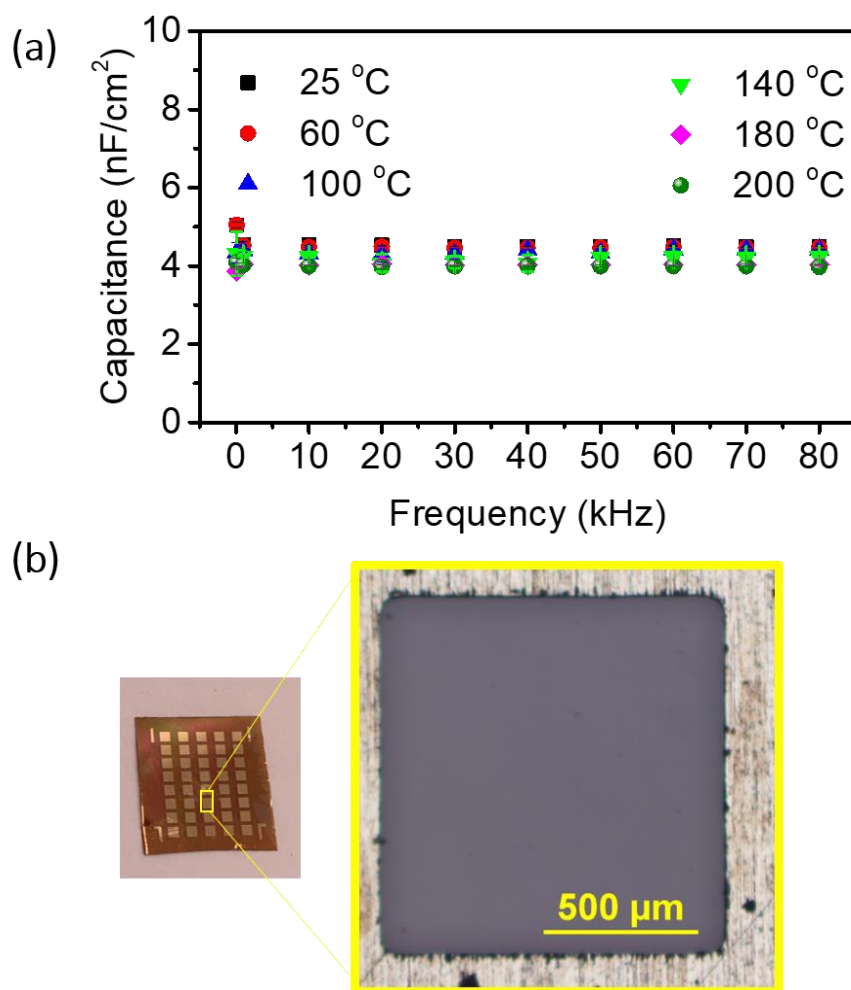


Figure S2. (a) Temperature-dependent capacitance measurement: the capacitance was first calculated to be around 4.5 nF/cm² when 1.1mm x 1.1mm shadow masks (b) were used to make to attain the Au/PI/Au sandwiched configuration. In-situ temperature-dependent measurements revealed that the PI layer can retain excellent capacitive properties even under baking conditions. The capacitance only showed to decrease from 4.5 to 4.1 nF/cm² when measured from room temperature to 200 °C.

3) Morphology optimization in the semiconducting thermally stable polymer blend

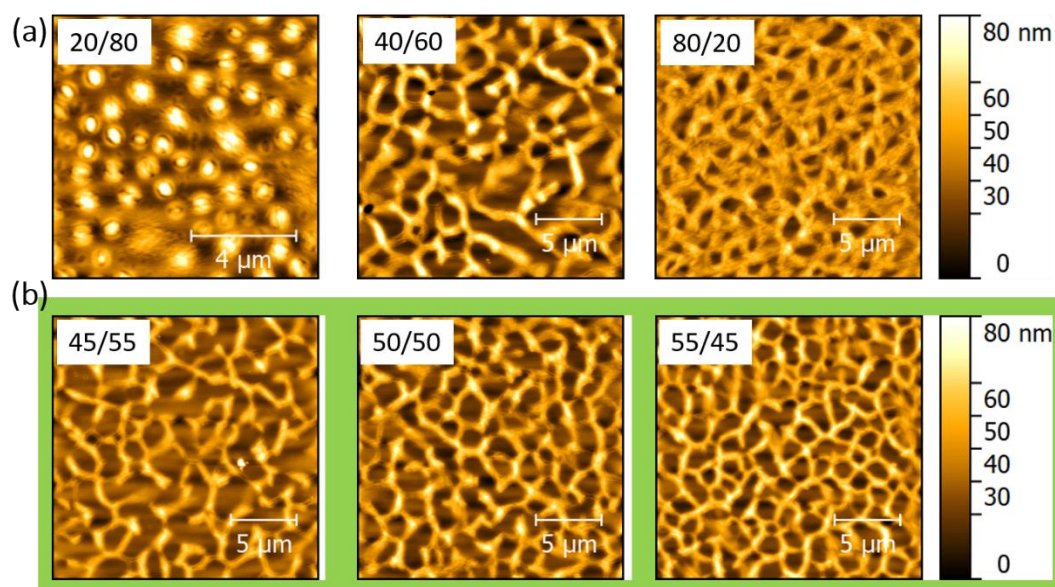


Figure S3. Morphology optimization in PII-2T/Matrimid blend films. The AFM height images show the evolution of the interpenetrating bi-continuous morphology when the w/t % of PII-2T/Matrimid was varied from 20/80 to 80/20. The bi-continuous morphology was found when as high as 40 w/t % of the conjugated polymer was added in the blend. The 50/50 blend films were selected for the temperature-dependent studies.

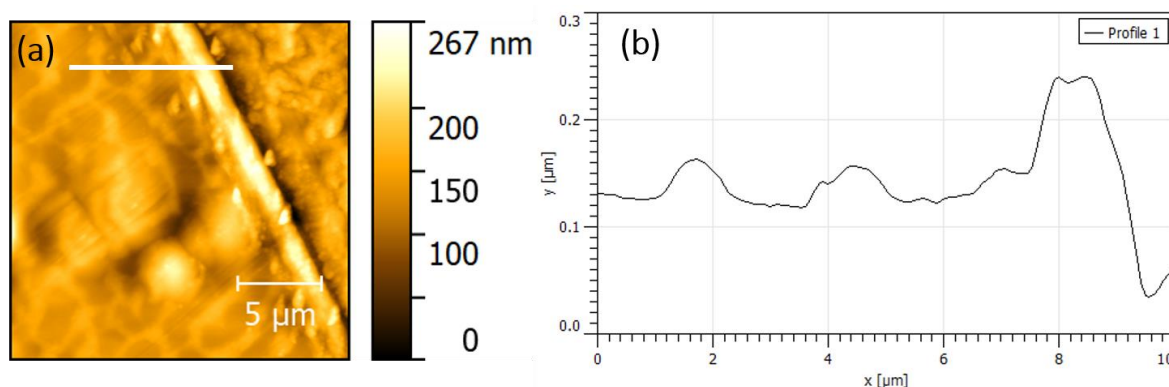


Figure S4. Thickness extraction of PII-2T film. The AFM height image was retaken after a notch was gently created through the film atop of the tougher cured PI layer. Note the accumulation of the material upon cutting which renders the image quality less appreciable. The extracted thickness was found to be around 120 nm (± 15 nm).

4) Transistor devices dimensions and characterization

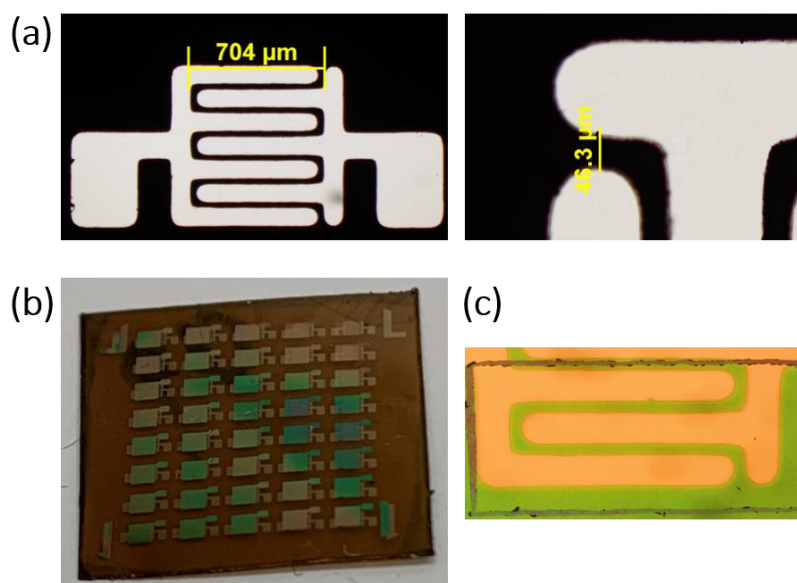


Figure S5. Optical micrographs of (a) the steel shadow masks used for metal deposition and (b), (c) the plastic devices. For mobility extraction a channel width of 1500 μm was carefully isolated using a sharp probe tip.

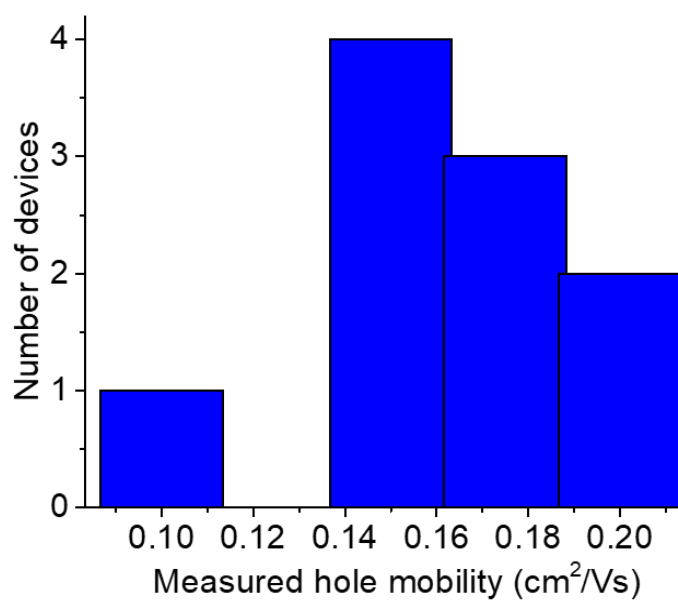


Figure S6. Statistical distribution of extracted mobility values from 10 representative devices fabricated from the 50/50 blend films. On average, hole mobility of 0.15 cm^2/vs could be attained.

5) Hysteresis and leakage current evaluation

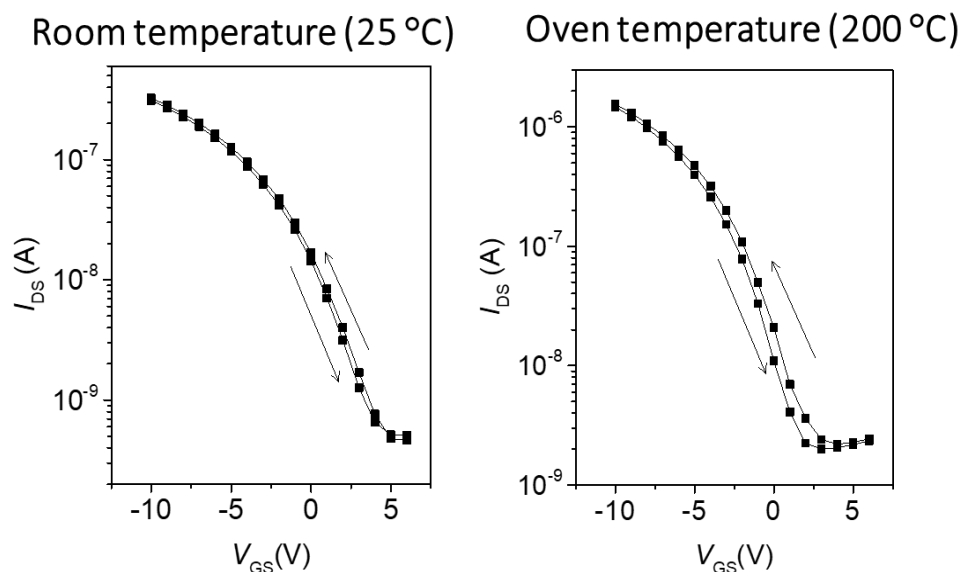


Figure S7. Characteristic transfer curve showing the forward and backward scan. Low hysteresis is observed in the polyimide-based devices. The V_{DS} is kept to -10 V.

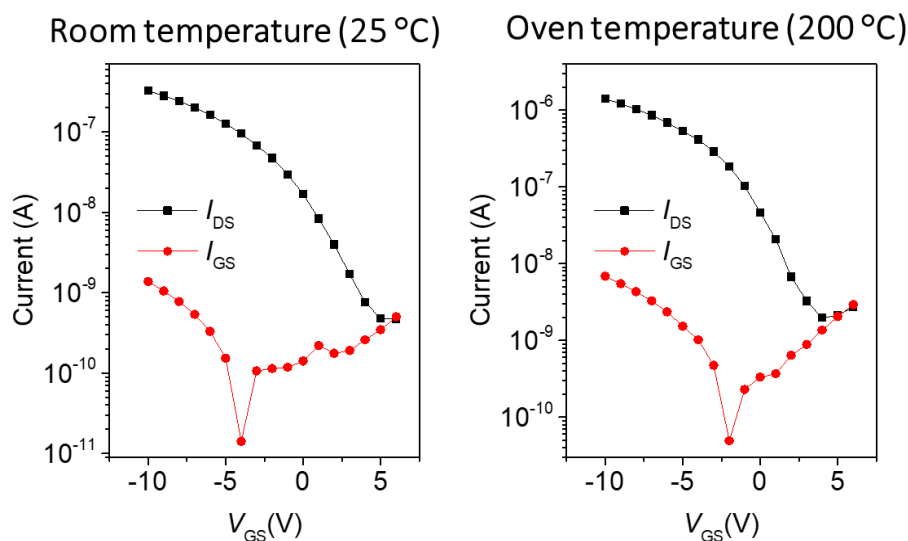


Figure S8. Temperature-dependent source to drain and source to gate currents from the plastic device. Low gate current is observed indicative of excellent capacitive properties and overall devices stability even under baking conditions. The V_{DS} is kept to -10 V.

6) Temperature-dependent FETs characterization

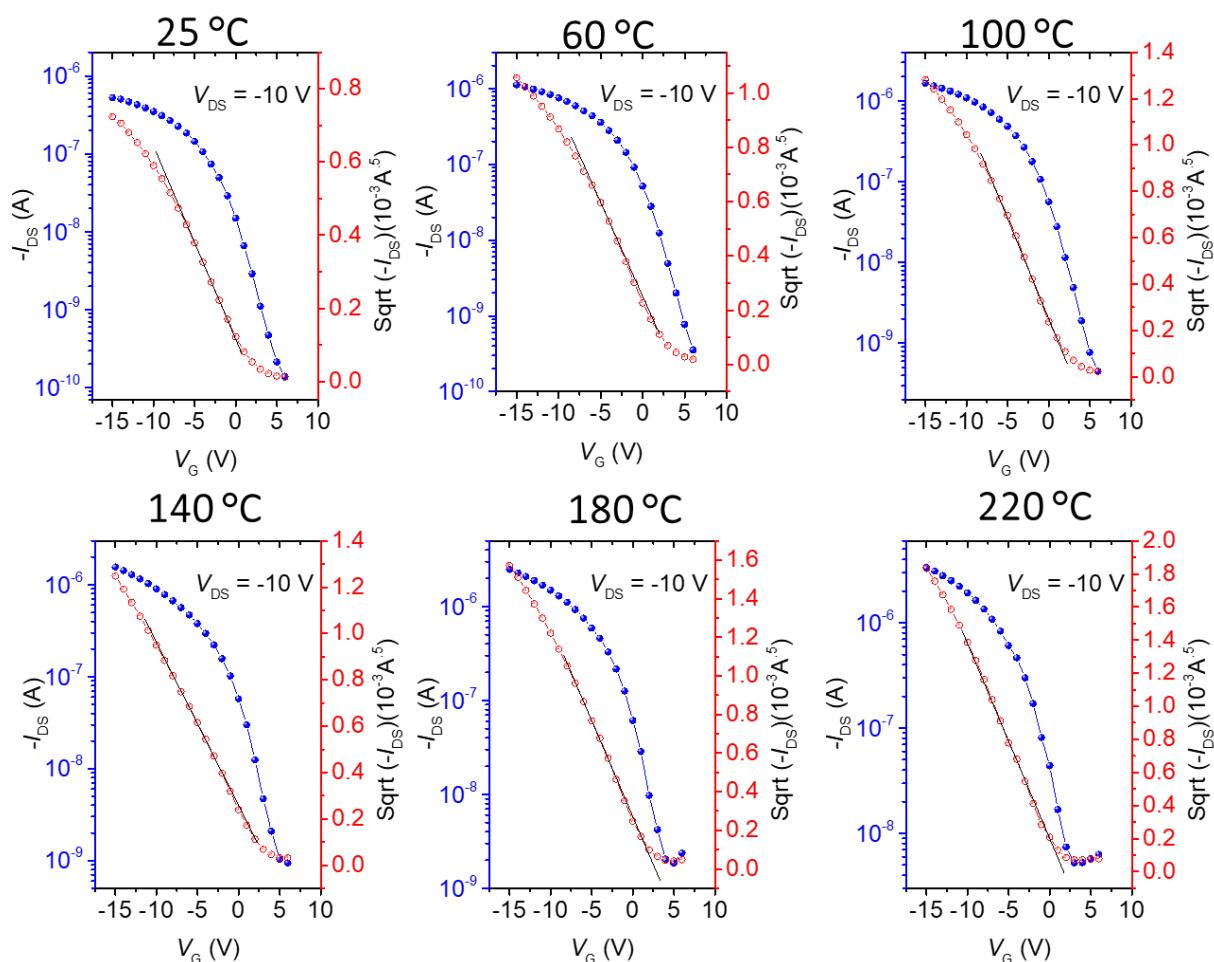


Figure S9. Characteristic transfer curves of devices measured at different operation temperatures in the open air. The plastic transistors can retain ideal characteristics and low power consumption at extremely elevated temperatures. For each temperature set point, the devices were allowed to reach a thermal equilibrium for at least 20 minutes before the measurement.

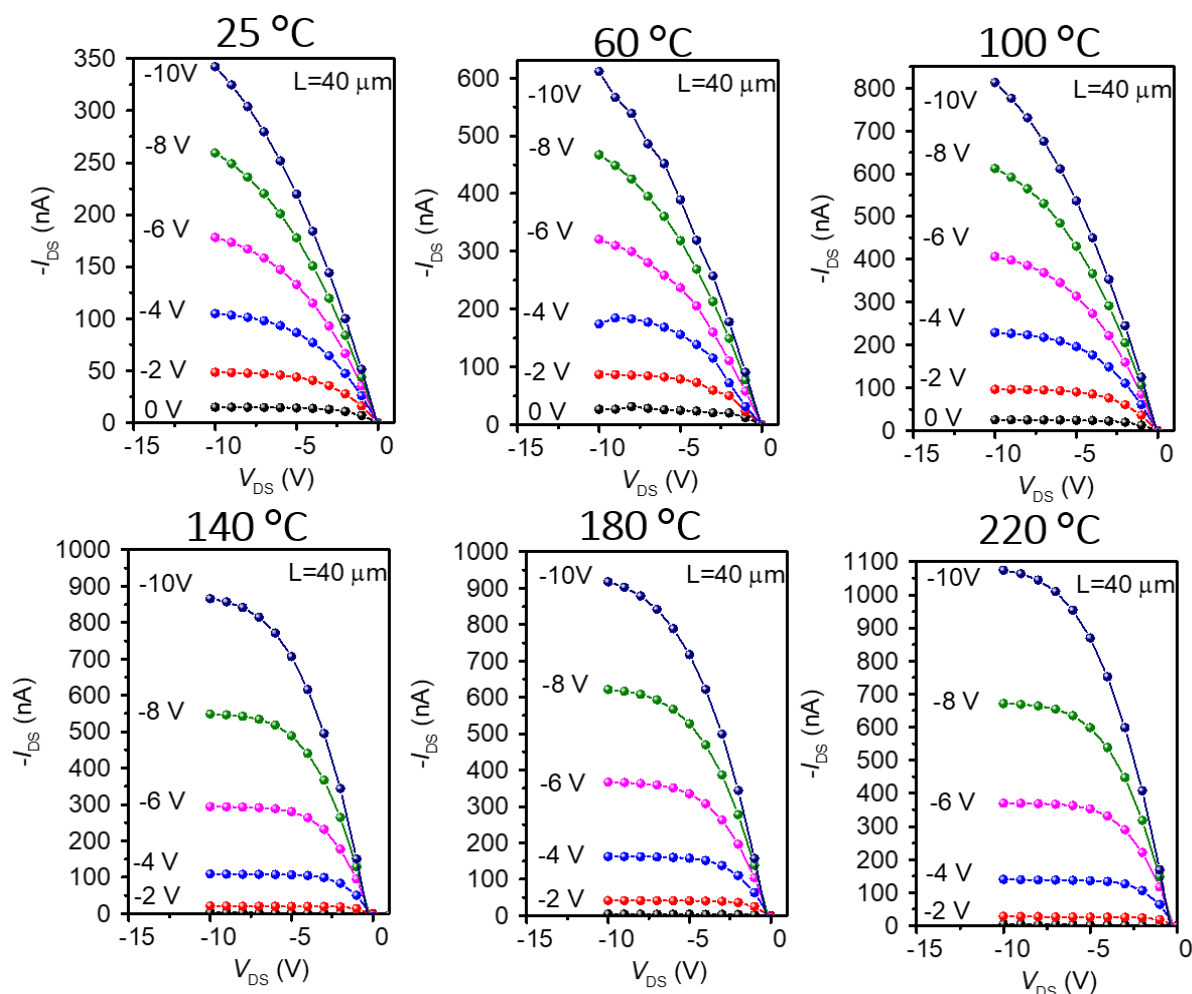


Figure S10. Characteristic output curves of devices measured at different operation temperatures in the open air. The current shows to increase steadily with increasing operating temperature and to remain stable at all temperatures.

References

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